IN THE CLAIMS

1. (Currently amended) A method of forming a ferroelectric memory device, comprising:

preparing a semiconductor substrate comprising an interlayer dielectric layer and a capacitor lower electrode contact formed through the interlayer dielectric layer;

forming a cylindrical capacitor lower electrode on the interlayer dielectric layer, the lower electrode coupled to ~~thereby covering~~ the contact;

conformally stacking a ferroelectric layer by using a chemical vapor deposition (CVD) technique over substantially the entire surface of the semiconductor substrate including the capacitor lower electrode; ~~and~~

forming a capacitor upper electrode in the shape of a spacer surrounding the sidewall of the ferroelectric layer; and

forming a plate line over a region of the semiconductor substrate where the upper electrode is formed, the plate line being in electrical contact with the upper electrode.

2. (cancelled)

3. (Currently amended) The method as claimed in claim ~~2~~ 1 in which plural ones of such capacitors are arranged across the semiconductor substrate surface, after forming the upper electrode and before forming the plate line, further comprising:

stacking an insulation layer over substantially the entire surface of the semiconductor substrate, to partially fill gaps between the capacitors,

the insulation layer exposing at least a part of the upper electrode.

4. (Original) The method as claimed in claim 3, wherein:

the recessing of the insulation layer is performed by an etching process; and

the etching process uses an etch gas including at least one gas selected from a group consisting of CHF_3, CF_4, Ar, and N_2 to make the insulation layer have etch selectivities with respect to the upper electrode and the ferroelectric layer.

5. (Original) The method as claimed in claim 1, wherein the forming of the lower electrode further comprises:

sequentially stacking a lower electrode layer and a hard mask layer over substantially the entire surface of the semiconductor substrate;

forming a hard mask pattern through photolithography and etching processes with respect to the hard mask layer; and

etching the lower electrode layer by using the hard mask pattern as an etch mask to form the lower electrode.

6. (Original) The method as claimed in claim 5, further comprising;

stacking a conductive adhesive assistant layer before stacking the lower electrode layer, wherein the adhesive assistant layer is patterned together with the lower electrode layer.

7. (Original) The method as claimed in claim 1, wherein the forming of the lower electrode comprises:

forming a sacrificial layer at the semiconductor substrate;

forming a contact hole at the lower electrode region of the sacrificial layer;

filling the contact hole with a conductive layer; and

removing a remnant part of the sacrificial layer.

8. (Original) The method as claimed in claim 7, wherein the filling of the contact hole is performed by an electroplate technique.

9. (Original) The method as claimed in claim 1, wherein:

the forming of the upper electrode further comprises stacking an upper electrode layer at the entire surface of the semiconductor substrate and anisotropically etching the entire surface of the upper electrode to expose the ferroelectric layer; and

the anisotropical etching of the upper electrode layer uses an etch gas including oxygen and a combination gas composed of at least one gas selected from a group consisting of Cl_2, BCl_3, HBr, and Ar, to make the upper electrode layer have an etch selectivity with respect to the ferroelectric layer.

10. (New) A method of forming a ferroelectric memory device, the method comprising:

preparing a semiconductor substrate including an interlayer dielectric layer;

forming a contact plug in the interlayer dielectric layer;

stacking a lower electrode layer covering the contact plug;

forming a hard mask layer on the lower electrode layer;

patterning the hard mask layer and lower electrode layer to form a cylindrical lower electrode correspondingly covering the contact plug;

conformally stacking a ferroelectric layer substantially over the entire surface of the semiconductor substrate;

conformally stacking an upper electrode layer over the ferroelectric layer;

etching the upper electrode layer to form a spacer shaped upper electrode surrounding the vertical sidewalls of the lower electrode with the ferroelectric layer disposed between the upper and lower electrodes;

stacking a conductive layer over substantially the entire semiconductor substrate; and

patterning the conductive layer to form a plate line over a region of the semiconductor substrate where the upper electrode is formed, the plate line being in electrical contact with the upper electrode.

11. (New) The method of claim 10, further comprising before stacking the lower electrode layer, stacking a conductive adhesive assistant layer covering the matrix of contact plugs.

12. (New) The method of claim 12, wherein the conductive adhesive assistant layer may be one selected from a group of titanium, titanium nitride, titanium aluminum nitride (TiAlN), titanium silicide, or titanium silonitride (TiSiN).

13. (New) The method of claim 11, further comprising after stacking the conductive adhesive assistant layer, stacking an additional conductive barrier layer.

14. (New) The method of claim 10, further comprising before stacking the conductive layer over substantially the entire semiconductor substrate:

stacking a nonconductive material layer over substantially the entire surface of the semiconductor substrate; and

etching the nonconductive material layer such that the ferroelectric layer and a top part of the spacer shaped upper electrodes are exposed.

15. (New) A method of forming a ferroelectric memory device comprising:

preparing a semiconductor substrate including an interlayer dielectric layer;

forming a matrix of contact plugs in the interlayer dielectric layer;

forming a sacrificial oxide layer on the interlayer dielectric layer;

forming a matrix of node holes in the sacrificial oxide layer over each of the contact plugs;

filling the matrix of node holes with a lower electrode material by using an electroplating method;

forming a matrix of cylindrically shaped lower electrodes over each of the contact plugs by removing the sacrificial oxide layer;

conformally stacking a ferroelectric layer substantially over the entire surface of the semiconductor substrate;

conformally stacking an upper electrode layer over the ferroelectric layer;

etching the upper electrode layer to create memory cells by creating spacer shaped upper electrodes surrounding the vertical sidewalls of the lower electrodes with the ferroelectric layer disposed between the upper and lower electrodes;

stacking a conductive layer over substantially the entire semiconductor substrate; and

patterning the conductive layer to form lines connecting upper electrodes of cells composing a row or column of a memory cell matrix.